REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claims 1-16 were presented for consideration in this application. By the foregoing amendment, Applicant has amended Claims 1, 7, 14 and 15. Claim 8 has been canceled. Claims 1-7 and 9-16 are now pending.

Applicant thanks the Examiner for noting "applicant has not filed a certified copy of the applications as required by 35 U.S.C. 119(b)." Applicant sent certified copies on 3/11/2003 which should now be on file.

Applicant has updated serial numbers on page 1 of the specification, and amended paragraphs 52 and 73 as requested.

Applicant has amended Claim 7 as requested to correct an informality.

Rejections

Claims 1-3, 5-6, 8-9, 11, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Bausch (6.339,816).

Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch in view of Slater, "A Guide to RISC Microprocessors".

Claims 7, 10, and 12-13 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Bausch.

Applicant has amended Claim 1 to include the limitation of Claim 8 and therefore canceled Claim 8. Regarding Claim 8, the Examiner states:

> Bausch teaches that if control bit GL is set, then all entries that relate to global user pages must be declared invalid. See column 3, lines 1-3. A single command would be used to generate this invalidation process.

Applicant respectfully disagrees with this characterization of Bausch. Bausch does teach that in order to restore the write protection managed by SW (exception mechanism), entries with their "D" bit and "GL" bit set must be declared invalid". (Col 3, lines 1-11) Bausch **does not say HOW**. There are multiple ways of invalidating entries. Upon a full reading of the R4000 User's

Manuel, second edition, Applicant believes the only available solution would be to read each entry of the TLB through the TLBR instruction, check the G bit or the ASID field, and invalidate the line through a write entry with index according to the need. Obviously, this takes a number of commands and significant time. Irregardless, the Examiner has provided no support for the assertion that "A single command would be used to generate this invalidation process."

Applicant's innovation provides for "invalidating a portion of the plurality of translated memory address in the TLB in a manner that is qualified by the shared indicator in response to only a single command issued from the processor" as recited in amended Claim 1. This innovation provides a much improved efficiency for TLB maintenance. Bausch does not suggest providing a single command for invalidating a portion of the TLB. Claim 1 is therefore allowable over Bausch.

Dependent Claims 2-7 and 9-12 depend directly or ultimately on an allowable base Claim and are therefore allowable for this reason and by virtue of their further distinctive recitations. For example, Claim 5 recites "wherein the step of invalidating is qualified by both the shared indicator and the task identification value." Bausch does suggest "entries of the corresponding task must be declared invalid" and indicates "this is accomplished in a simple manner by modifying the addresses space identifier (ASID) that is allocated to the task." (Col. 3, lines 4-11) However, changing the ASID does not cause "invalidating a portion of the plurality of translated memory address in the TLB" as recited in depended upon Claim 1. Therefore, Bausch does not suggest the operation recited by Claim 5 as it depends on Claim 1 and Claim 5 is therefore allowable over Bausch for this further reason.

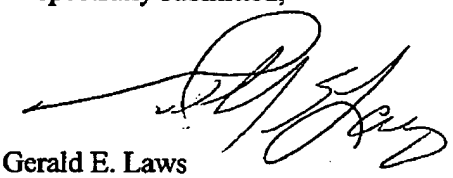
Claim 7 recites: "wherein the second qualifier value identifies which of the plurality of processors requested the respective translated memory address." The Examiner admits Bausch does not suggest multiprocessor operation. Applicant disagrees that it would be obvious to combine Applicant's innovative method of invalidating shared/non-shared TLB entries in a multi-processor system where multiple processors share TLB entries, since multiprocessor systems tend to have a separate TLB associated with each processor. Claim 7 is therefore allowable over Bausch for this additional reason.

Independent Claim 14 has been amended slightly to clarify that a single operation command is used to "invalidate all entries having a specified value in the shared indicator field." This claim is allowable over Bausch for the reasons discussed above with regard to amended Claim 1. Claims 15-16 depend on allowable independent Claim 14 and are therefore allowable for this reason and by virtue of their further distinctive recitations.

Applicant believes this application and the claims herein to be in a condition for allowance and respectfully requests that the Examiner allow this application to pass to the issue branch.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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